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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,931	08/18/2003	Hassan Tanbakuchi	10020832-1	3861

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AGILENT TECHNOLOGIES, INC.
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EXAMINER	
BOUTSIKARIS, LEONIDAS	
ART UNIT	**PAPER NUMBER**
2872	

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,931	TANBAKUCHI, HASSAN	
	Examiner	Art Unit	
	Leo Boutsikaris	2872	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parayanthal (US 6,057,954) in view of Miller (US 6,677,830) and Akiyama (US 2003/0138179).

Regarding claim 1, Parayanthal discloses an electro-absorption modulator device (Fig. 2), whose electrical equivalent circuit is shown in Fig. 3. The device comprises an input wire 214 and an output wire 216, each having a series inductance L1 and L2, respectively, and a resulting characteristic impedance at the operating frequency. Furthermore, the device comprises an electro-absorption modulator having a signal electrode 206, a shunt capacitance C, and a resulting characteristic impedance at the operating frequency; wherein the values of the various inductances, capacitances and resistances are chosen so that the characteristic impedance of the device is substantially matched to the target source impedance R1 at the target operating frequency (lines 6-39, col. 3, 63-65, col. 3).

Regarding the values of the impedances of the input and output wires (due to L1 and L2, respectively) as well as the impedance of the modulator itself (due to Rs and C), Parayanthal discloses sets of experimental results, wherein the reflection coefficient is measured for various

values of the electrical components. In one example, Rs was 15 ohms, C was 0.7 pF, which resulted in an impedance for the modulator itself having magnitude of 27.2 Ohms (see second term of equation (1)), at an operating frequency of 10 GHz, which is less than the target source impedance of 50 Ohms (lines 61-67, col. 5). Similarly, the magnitude of the impedance due to L2, at the same frequency, for L2=2 nH, is 125.6 Ohms, which is greater than the source impedance of 50 Ohms. Regarding the impedance due to L1, Fig. 10B shows a contour plot of the device return loss coefficient, wherein a range of values of L1 which would produce a characteristic impedance greater than 50 Ohms (at a target operating frequency of 10 GHz, for example) is shown (for example L1 > 0.8 nH).

However, in Parayanthal's device, wires are used to connect the modulator with the modulating source and a load resistor, instead the claimed microstrip lines. Miller discloses an optical electroabsorption modulator integrated device (Fig. 1), wherein a microstrip line 12 is used to connect the modulator 10 with the modulator source 26 (line 57, col. 2 to line 6, col. 3). The purpose of the microstrip line is to provide additional impedance so that there is impedance matching between the external signal source 26 and the modulator 10 (lines 1-5, col. 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace or add to the electrical wires in Parayanthal device microstrip lines, as taught by Miller, for achieving better impedance matching in the circuit, since it is easier to change the inductance of a microstrip line because of its distributed nature.

In addition, Parayanthal does not specify the length of the microstrip lines and the signal electrode being less than a one-quarter of the target wavelength corresponding to the target operating frequency. Akiyama discloses an electro-absorption modulator device (Fig. 8)

comprising various segments of modulating elements 10A, each having a signal electrode 8b, and adjacent modulating elements being connected with microstrip lines 8a. The length of all the above elements is preferably less than a quarter of the wavelength of the high frequency electric input signal (i.e., the modulation signal), see [0091], [0097]-[0102], [0110]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the lengths of all the components of the device disclosed by Parayanthal smaller than one quarter of the wavelength corresponding to the operating frequency, as taught by Akiyama, for maintaining the overall impedance of the device small and matched to the input impedance of 50 Ohms (see [0091] and [0125] in Akiyama).

Regarding claim 5, the input inductance L1 is chosen so that the device circuit has a characteristic impedance close to the target operating frequency (i.e., producing small return loss).

Regarding claims 6-9, 13-17, Parayanthal does not disclose that the signal electrode may be segmented, comprising multiple spaced-apart signal electrode segments connected in series, with adjacent segments being connected by a respective microstrip line. In Akiyama's electro-absorption modulator device, the signal electrode has a distributed traveling wave structure comprising multiple spaced-apart segments 8b connected via wires 8a. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a segmented signal electrode for the modulator of Parayanthal, as taught by Akiyama, for achieving smaller reflection of high frequency electric signals due to mismatch of impedances (see [0032]-[0033] in Akiyama), while replacing the wires 8a with microstrip lines, as taught by Miller.

Regarding claim 10, the target source impedance is 50 Ohms.

Regarding claim 12, Parayanthal does not specify that the signal electrode is formed on a ridge structure, i.e., that the waveguiding core layer has a ridge structure. In Akiyama's electro-absorption modulator device, the modulation occurs along an optical waveguide core layer 103b has the form of a ridge (see Fig. 11 and [0118]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the modulator in the device of Parayanthal in the form of a ridge, as taught by Akiyama, for better confinement of the light guided therein.

Regarding claim 11, there are electrically insulating layers 6 disposed between electrically conducting layers 2 and 10A (see fig. 8 in Akiyama).

Claims 2-3, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parayanthal (US 6,057,954) in view of Miller (US 6,677,830) and Akiyama (US 2003/0138179) and further in view of Mayer (US 5,793,516).

Parayanthal in view of Miller and Akiyama discloses all the limitations of the above claims except for disclosing that a shunt capacitance is connected in conjunction with the input and output inductances (constituting the input and output microstrip lines). Mayer discloses an optical modulator circuit, wherein in one embodiment, LC elements are connected at the input and output of the modulator element (i.e., L1 and C1 at the input of MD and L2 and C2 at the output of MD). It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect shunt capacitances to the input and output inductances in the device of Parayanthal, for performing filtering for high frequency modulation signals.

Regarding claim 3, the values of the inductances and capacitances are chosen so that the modulator circuit impedance substantially matches the source impedance at the operating frequency (lines 40-65, col. 3 in Parayanthal).

Claims 4, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parayanthal (US 6,057,954) in view of Miller (US 6,677,830), Akiyama (US 2003/0138179) and Mayer (US 5,793,516) and further in view of Nagra (US 6,590,691).

Parayanthal in view of Miller, Akiyama and Mayer discloses all the limitations of the above claims except for disclosing a parallel RC circuit at the output of the modulator. Nagra discloses an optical modulator device 200, wherein a parallel RC circuit 208 is disposed after the output series inductance, which is disposed after the modulator element 202 (Fig. 5, line 58, col. 7 to line 11, col. 8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect a shunt capacitance in parallel with the output resistive bonding pad, as taught by Nagra, for filtering high frequency signal components.

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Leo Boutsikaris whose telephone number is 571-272-2308.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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August 4, 2005

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